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High-Temperature Stable Operation of Nanoribbon Field-Effect Transistors

Chang-Young Choi · Ji-Hoon Lee · Jung-Hyuk Koh · Jae-Geun Ha · Sang-Mo Koo · Sangsig Kim

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Abstract We experimentally demonstrated that nanoribbon field-effect transistors can be used for stable high-temperature applications. The on-current level of the nanoribbon FETs decreases at elevated temperatures due to the degradation of the electron mobility. We propose two methods of compensating for the variation of the current level with the temperature in the range of 25–150°C, involving the application of a suitable (1) positive or (2) negative substrate bias. These two methods were compared by two-dimensional numerical simulations. Although both approaches show constant on-state current saturation characteristics over the proposed temperature range, the latter shows an improvement in the off-state control of up to five orders of magnitude (-5.2×10^{-6}).

Keywords Field-effect transistors (FETs) · Electron mobility · Variation of the current level · Nanoribbon FET

Introduction

The nanoribbon structure has recently been extensively investigated for many applications, such as ZnS nanoribbon lasers [1], graphene nanoribbon field-effect transistors (GNRFETs) [2], nanoribbon sensors in Si [3] and other materials [4]. Nanoribbon structures offer a relatively easy system to access, control and process, due to their relatively larger scale compared to other nanostructures, such as nanowires (NWs) [5], nanodots (NDs) [6] and nanotubes (NTs) [7]. Nanoribbons or thin silicon on insulators have many advantages, such as low leakage and a high on/off current ratio, I_{ON}/I_{OFF}, which leads to low power consumption while the device is inactive [8]. In addition, since their parasitic capacitance is effectively eliminated by the underlying insulating layer, nanoribbon- or thin silicon-based devices have advantages for RF applications [9]. Such structures also have a lower threshold shift in response to temperature variations [10–13]. However, the reduction in mobility induced by the thermal scattering causes the operation points of the device to vary with the temperature. This temperature-dependent variation of the operation points makes the devices hard to operate properly. [14] For some high-temperature circuits, it is desirable that the individual devices have a specific operation point where the device characteristics show no variation with temperature. In this work, we demonstrate the feasibility of the constant operation of the fabricated devices in the temperature range from 25 to 150°C. The method employed to achieve the constant operation of the fabricated devices, which is similar to zero temperature coefficients (ZTC), is based on the use of a substrate bias (V_{SUB}). By accumulating or depleting the carriers on the channel surface using the substrate bias (V_{SUB}), we show that the device on/off characteristics show minimal variation with temperature.

Experimental

A 30-nm-thick p-type silicon on insulator (SOI) wafer has been used as the starting material, and the SOI layer has

C.-Y. Choi · J.-H. Lee · J.-H. Koh · J.-G. Ha · S.-M. Koo (✉)
College of Electronics and Information Engineering, Kwangwoon University, Seoul 139-701, Korea
e-mail: smkoo@kw.ac.kr

S. Kim
Department of Electrical Engineering, Korea University, Seoul 136-701, Korea

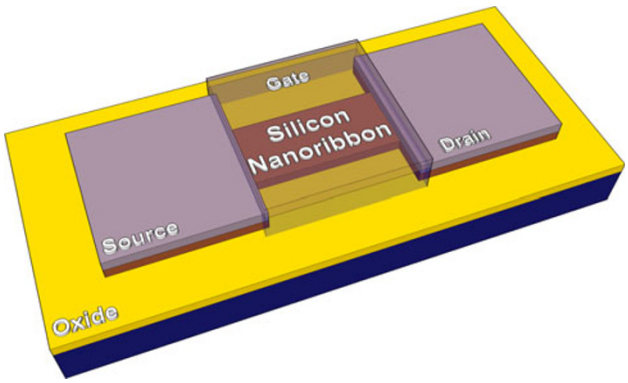

Fig. 1 Schematic cross-section of fabricated nanoribbon FET

been thinned down to 20 nm by oxidation. The length L_{CH} and width W_{CH} of the channels, defined by conventional lithography, were 30 and 10 μm, respectively. The thickness (t_{OX}) of the gate oxide was 40 nm, and n^+ poly silicon was used as the gate electrode. Au/Al was used as the metal electrodes for the source, drain, gate, and substrate contacts. Figure 1 shows a schematic representation of the fabricated nanoribbon device. The electrical characteristics of the devices were measured by an HP4155b semiconductor parameter analyzer with a hot chuck for elevated temperature measurements. To diffuse the heat over the whole device at each temperature, the device was heated for a long enough time before each measurement.

We used a substrate bias (V_{SUB}) to ensure the constant operation of the devices at elevated temperatures, and the measurements were compared with the two-dimensional simulation results obtained from structures identical to those of the fabricated devices [15]. In order to evaluate the substrate and top bias-dependent channel carrier modulation as a function of temperature, we extracted the channel cross-section profiles containing the on- and off-current density distribution at different temperatures.

Results and Discussion

Figure 2a shows the gate transfer characteristics of the fabricated (solid lines) and simulated (dashed lines) nanoribbon FET structures. The current level decreases as the temperature increases, which is ascribed mainly to the influence of lattice scattering caused by the elevated temperature on the mobility decay. Figure 2b shows the decays in the normalized saturation current level and mobility values at different temperatures. Both the simulated and measured current levels and therefore the mobility values follow the power-law decay behavior ($\propto T^{-1.5}$). Note that the mobility values presented in Fig. 2 do not have a unit but instead show relative degradation ratio with respect to the room temperature value. Such mobility degradation, where lattice scattering is the dominant scattering mechanism, can be expressed by a power law [16]. This variation of the current level or mobility can make the device difficult to use in high-temperature or temperature-variable ambient applications.

To overcome such a thermal problem, which may result in the variation of the operation point, it is desirable to keep the current level constant over a range of temperatures. In order to realize such operation of the nanoribbon FETs, we propose the following two methods of compensating for the variation in the current level with temperature from room temperature up to 150°C; (1) A suitable positive bias V_{SUB} is applied to realize this constant level operation, by enhancing the current level at elevated temperatures to the room temperature ($T \sim 25$°C) current level, as can be seen in method '(1)' of Fig. 3a. (2) A negative V_{SUB} is applied to reduce the current level at different temperatures down to its level at $T \sim 150$°C, as can be seen in method '(2)' of Fig. 3a.

Figure 3a shows the drain characteristics of the fabricated (solid lines) and simulated (dashed lines) nanoribbon FETs as a function of temperature in the range between 25 and 150°C. Figure 3b, c, d and e show the channel cross-sections of the device, showing the conduction current

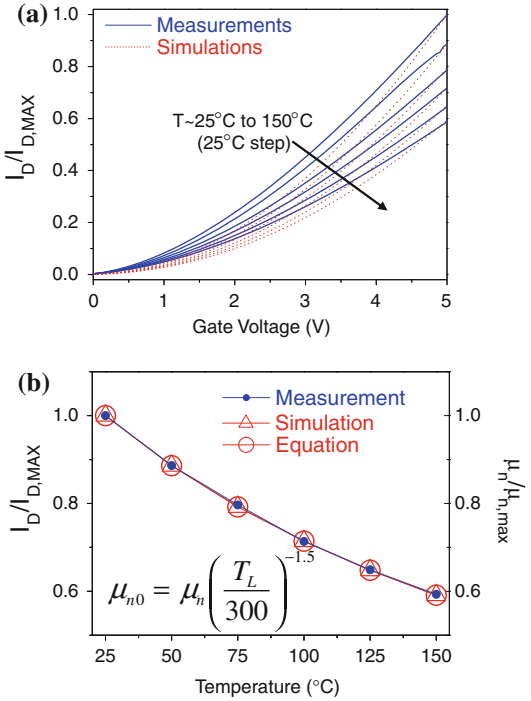

Fig. 2 **a** Measured (*solid line*) I_{DS}—V_{GS} curves for the fabricated Si nanoribbon FETs. (The *dashed lines* show the corresponding results obtained from the 2D numerical simulations). **b** The power law decay behavior of the normalized drain current and mobility as a function of temperature in the range from 25 to 150°C

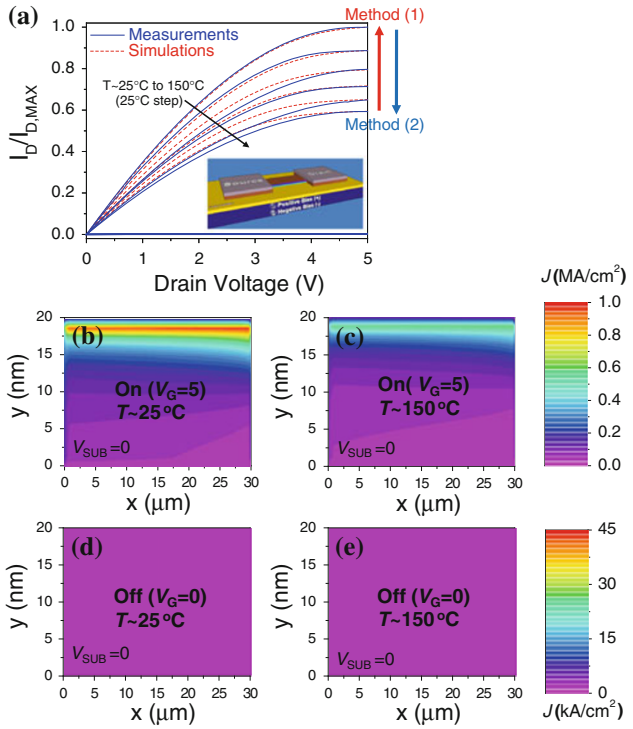

Fig. 3 **a** Measured (*solid line*) I_{DS}—V_{DS} curves for fabricated Si nanoribbon FETs. (The *dashed lines* show the corresponding results obtained from the 2D numerical simulations). **b**–**e** show the channel cross-sections of the device, indicating the conduction current density contours for the 'on' state **b** at room temperature and **c** $T = 150$°C with $V_{SUB} = 0$, and for the 'off' state **d** at room temperature and **e** $T = 150$°C with $V_{SUB} = 0$

density contours. Figure 3b and c show the conduction current density contours for the 'on' state at room temperature and $T \sim 150$°C, respectively. These two contour plots clearly indicate that the conduction current is reduced by the mobility degradation as the temperature increases. Figure 3d and e show the constant 'off' states at room temperature and $T \sim 150$°C, respectively.

Figure 4a shows the compensated I_{DS}—V_{DS} curves derived from the measurements (solid lines) and simulations (dashed lines) with a positive substrate bias V_{SUB}, according to 'method (1)'. The inset shows the V_{SUB} values applied for the purpose of keeping the operation of the device constant for temperatures in the range from 25 to 150°C. An approximately constant level on-state was maintained in spite of the temperature variation. However, the maximum leakage current in the off state is as much as ~9% of the on-state current level. This is due to the additional inversion currents on the bottom of the channel surface formed by the positive substrate bias, V_{SUB}. As can be seen in Fig. 4c, an increase in the current density, J, is clearly observed on the bottom of the channel surface.

Unlike in method (1), where the complete off-state of the device is not achieved, method (2) uses a negative substrate bias, V_{SUB}. Figure 5a shows the compensated I_{DS}—V_{DS} curves of the fabricated (solid lines) and simulated (dashed lines) devices with negative substrate bias (V_{SUB}) based on method (2). The inset also shows the negative substrate bias (V_{SUB}) applied for the purpose of keeping the operation of the device constant for temperatures in the range from 25 to 150°C. Constant on- and off-states were successfully accomplished at different temperatures. In contrast to method (1), the off-state leakage current levels are drastically suppressed in the linear scale values of the drain currents. This is due to the negative V_{SUB}, which effectively depletes the carriers in the channel. This can also be seen in Fig. 5b and c, where no significant

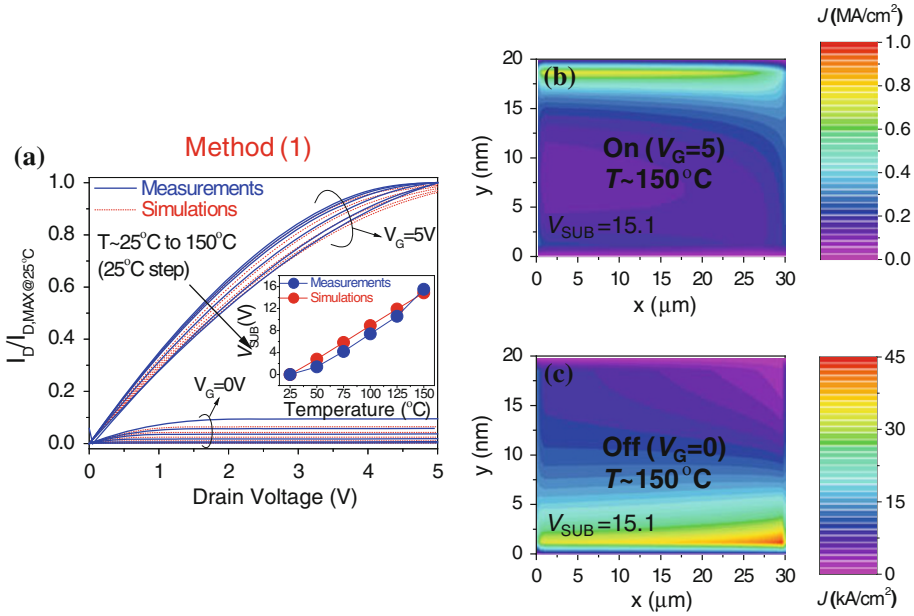

Fig. 4 **a** Compensated I_{DS}—V_{DS} curves with positive substrate bias (V_{SUB}) of the device. The inset shows the substrate bias (V_{SUB}) applied for the purpose of keeping the operation of the device constant for temperatures from 25 to 150°C. (The *dashed lines* show the corresponding results obtained from the 2D numerical simulations.) **b** and **c** show the channel cross-sections of the simulated device, indicating the conduction current density contours for the compensated **b**'on state' and **c**'off state' with $V_{SUB} = 15.1$ V at $T = 150$°C

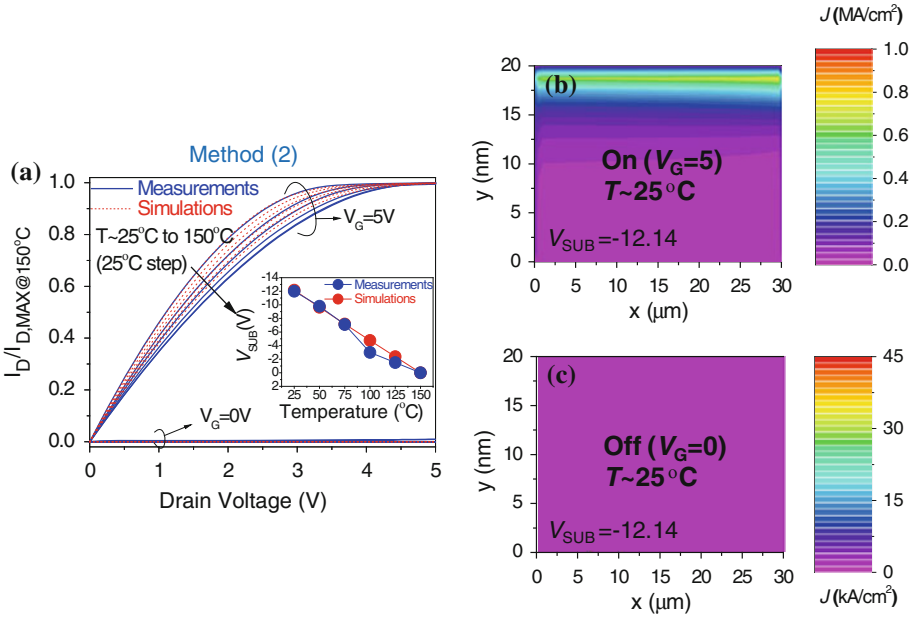

Fig. 5 **a** Compensated I_{DS}—V_{DS} curves with negative substrate bias (V_{SUB}) of the device. The inset shows the substrate bias (V_{SUB}) applied for the purpose of keeping the operation of the device constant for temperatures from 25 to 150°C. (The *dashed lines* show the corresponding results obtained from the 2D numerical simulations.) **b** and **c** show the channel cross-sections of the simulated device, indicating the conduction current density contours for the compensated **b**'on state' and **c**'off state' with $V_{SUB} = -12.14$ V at $T = 150$°C

Table 1 Measured data shown as portion of leakage current levels (I_{LEAK}/I_{ON}) in percentages (%) at different temperatures

Temperature (°C)	Method 1 (%)	Method 2 (%)
25	0.28	5.2×10^{-6}
50	0.72	2.5×10^{-6}
75	1.9	2.8×10^{-5}
100	3.8	3.2×10^{-3}
125	5.8	9.8×10^{-3}
150	9.8	0.90

inversion currents are observed on the bottom of the channel surface.

Table 1 compares the off-state drain leakage portion of the two methods at different temperatures. As shown in Table 1, in the case of method (1), the off-state leakage portion measured at 25°C is 0.28%, whereas method (2) shows clearly reduced values of 5.2×10^{-6}, suggesting that the leakage control is about five orders of magnitude better than that in method (1). As the temperature increases, the leakage portion increases in both cases, but the leakage portion in method (2) is still one or two orders of magnitude smaller than that in method (1) at elevated temperatures of 125 and 150°C.

Conclusions

In summary, we report the constant temperature operation of nanoribbon FETs in the temperature range of 25–150°C. In order to compensate for the variation in the current level with the temperature in the range from 25 to 150°C, we propose two methods. The physical mechanisms are; (1) to accumulate the lower part of semiconducting channel by applying a suitable negative substrate bias to enhance the total current level at elevated temperatures or (2) to deplete the lower part of the semiconducting channel by applying a positive substrate bias to reduce the total current level at lower temperatures. The leakage current level was drastically reduced by the negative substrate bias, as the carriers in the channel are effectively depleted, thus compensating for the fluctuating off-current level. Although both approaches show constant on-state current saturation characteristics over the proposed temperature range, the latter shows an improvement in the off-state control of up to five orders of magnitude ($\sim 5.2 \times 10^{-6}$). These results were confirmed by two-dimensional numerical simulations, which show that the substrate bias causes the channel to be effectively depleted or accumulated.

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