

High Speed Capacitor-Inverter Based Carbon Nanotube Full Adder

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Abstract Carbon Nanotube field-effect transistor (CNFET) is one of the promising alternatives to the MOS transistors. The geometry-dependent threshold voltage is one of the CNFET characteristics, which is used in the proposed Full Adder cell. In this paper, we present a high speed Full Adder cell using CNFETs based on majority-not (Minority) function. Presented design uses eight transistors and eight capacitors. Simulation results show significant improvement in terms of delay and power-delay product in comparison to contemporary CNFET Adder Cells. Simulations were carried out using HSPICE based on CNFET model with 0.6 V VDD.

Keywords Full Adder · Carbon nanotube · Carbon nanotube field effect transistor · High speed · High performance

Introduction

Technology progress in all areas of life has resulted in a need for small devices with higher operating speeds, and this is why extensive researches in these fields have been completed. Finding a suitable alternative is necessary since when MOS transistors continue to scale deeper, several device non-idealities appear and cause significant intrinsic device hurdles such as leakage, power and quantum effect [1]. Molecular devices are becoming promising alternatives

to the existing silicon technology. CNFETs are one of the molecular devices that avoid most fundamental silicon transistor restriction and have ballistic or near ballistic transport in their channel [2, 3].

In CNFETs, Carbon Nanotubes (CNTs) are used as transistor channel. While a CNT contact directly to source and drain, Schottky Barrier is made in their junctions; therefore, these transistors are called Schottky Barrier CNFET (SB-CNFET) (Fig. 1a). SB-CNFETs exhibit strong ambipolar characteristics that constrain usage of these transistors in conventional CMOS-like logic families. This contact limits the transconductance in the ON state, and thus I_{on}/I_{off} ratio becomes rather low [1]. Another type of CNFETs shown in Fig. 1b is doped in un-gated portions and has similar behavior to CMOS transistors; thus, this type is named MOSFET-Like CNFET. The features of MOSFET-Like CNFETs [4] are; unipolar characteristics dissimilar to Schottky-Barrier transistors, more scalability in comparison to SB-CNFET, reducing the OFF leakage current and having higher ON current in source-to channel junction because of absence of the Schottky Barrier. In this paper, we use the word CNFET instead of MOSFET-like device.

The CNFET threshold is dependant on the diameter of the CNT used as a channel, so with a suitable diameter, a transistor with desired threshold will be attained. With diameter D_{CNT} , CNFET threshold can be calculated by using (1), and formula (2) depict how CNT diameter can be calculated where N_1 and N_2 are chirality of CNT and a is the lattice constant equal to 2.49 Å

$$V_{TH} = \frac{0.42}{D_{CNT}(\text{nm})} V. \quad (1)$$

$$D_{CNT} = \frac{a\sqrt{N_1^2 + N_2^2 + N_1N_2}}{\pi} \quad (2)$$

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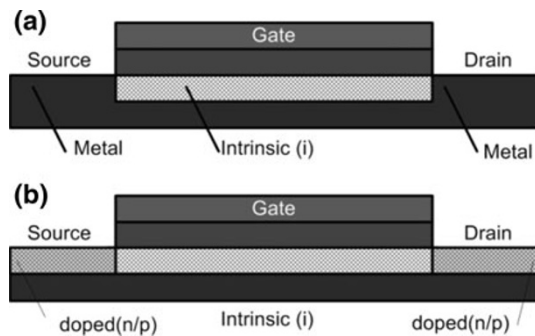


Fig. 1 Three possible types of CNTFETs **a** Schottky Barrier (SB) **b** Doped-S/D transistors

There are two methods by which new devices can be built using CNFETs; first one is by transporting existing logical functions directly to a new technology with replacing MOSFET with CNFET and the second one uses special properties of CNFETs to design entirely new circuit [4].

One of the important parts of the processor, which participates in many operations such as floating point computing and address generating [5], is Full Adders. Thus, increasing the performance of this part can improve total performance dramatically. There are standard implementations for Full Adder cells. Some of these implementations have used one logic style for the whole Full Adder and others that are hybrid Full Adders have used two or more logic style in a cell. Although they all have similar function, the way of designing intermediate nodes or the transistor count is varied. C-CMOS Full Adder cell uses one logic style [6] and is based on regular CMOS structure with conventional pull-up and pull-down transistors. The outputs are full swing, but with 28 transistors, it utilizes a large space in a chip. CPL is another Full Adder that uses one logic style. The outputs are full swing and make complementary outputs simultaneously, but the number of transistors used (transistor count) is 32 [7].

Many hybrid Full Adders are presented to date. In [8], hybrid Full Adder cells are categorized in three forms, XOR-XOR, XOR-XNOR and XNOR-XNOR adders and presented 24 transistor full swing Full Adder cell called Hybrid-CMOS Full Adder in XOR-XNOR form. The introduced adders [9, 10] are based on multiplexers, Full Adder presented in [9] uses 10 transistors, but the outputs are not full swing. Some adders are designed with majority function [11–15]. Majority function is a logic circuit that performs as a majority vote to determine the output of the circuit. This function has only odd numbers of input, and its output is equal to ‘1’ when the number of inputs ‘1’ is more than ‘0’. As depicted in (3), when this function has three inputs, it works like Carry-out in Full Adder, so with applying (4), the sum can be calculated

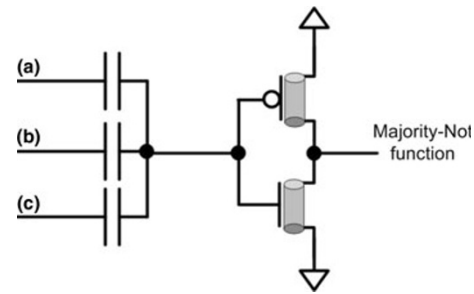


Fig. 2 Majority-not function

$$\text{Majority} = AB + AC + BC = \text{Cout} \quad (3)$$

$$\text{Sum} = \overline{\text{Cout}} \cdot (A + B + C) + ABC \quad (4)$$

Design [11] uses four transistors and seven capacitors and has full swing outputs. In [12], two Full Adders are presented using CNFETs in their designs, one used four CNFETs and seven capacitors and the other utilized only two transistors but two resistors employed caused an increase to the power dissipation. In next section, we exploit CNFET characteristics in order to introduce a new Full Adder that uses eight Carbon Nanotube transistors with eight capacitors, and it has full swing outputs. In Sect. 3, we will compare it with contemporary Full Adder based on Carbon Nanotube transistor with delay, power consumption and power-delay product criterions.

Proposed Full Adder

Majority-not (minority) function is a logic gate with odd numbers of inputs, and its output is high when the numbers of ‘1’s is less than the number of ‘0’s in the inputs of the gate. Fig. 2 presents a circuit used to implement minority function with inverter utilizing high- V_{TH} for both NMOS and PMOS. This circuit can be used to implement NAND gate using high- V_{TH} NMOS and low- V_{TH} PMOS, and NOR gate using low- V_{TH} NMOS and high- V_{TH} PMOS [15]. Formula (1) and (2) in previous section illustrate how the appropriate CNFET threshold voltage can be calculated. As shown in Fig. 3, in this paper for designing NAND and NOR function, we calculate the output SUM by formula (5)

$$\begin{aligned} \text{Sum} &= \text{Minority}(A, B, C, 2 * \text{Nand}(A, B, C), 2 \\ &\quad * \text{Nor}(A, B, C)) \\ &= \text{Minority}(A, B, C, \text{Nand}(A, B, C), \\ &\quad \text{Nand}(A, B, C), \text{Nor}(A, B, C), \text{Nor}(A, B, C)) \\ &= \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \overline{\text{Nand}(A, B, C)} \\ &\quad + \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \overline{\text{Nand}(A, B, C)} \cdot \overline{\text{Nor}(A, B, C)} \end{aligned}$$

$$\begin{aligned}
 & + \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \overline{\text{Nor}(A, B, C)} + \bar{A} \cdot \bar{B} \cdot \overline{\text{Nand}(a, b, c)} \\
 & + \bar{A} \cdot \bar{B} \cdot \overline{\text{Nand}(a, b, c)} \cdot \overline{\text{Nor}(A, B, C)} \\
 & + \bar{A} \cdot \bar{B} \cdot \overline{\text{Nor}(A, B, C)} + \bar{A} \cdot \bar{C} \cdot \overline{\text{Nor}(A, B, C)} \\
 & + \bar{A} \cdot \bar{C} \cdot \overline{\text{Nand}(A, B, C)} + \bar{A} \cdot \bar{C} \cdot \overline{\text{Nand}(A, B, C)} \cdot \overline{\text{Nor}(A, B, C)} \\
 & + \bar{B} \cdot \bar{C} \cdot \overline{\text{Nor}(A, B, C)} \\
 & + \bar{B} \cdot \bar{C} \cdot \overline{\text{Nand}(A, B, C)} + \bar{B} \cdot \bar{C} \cdot \overline{\text{Nand}(A, B, C)} \cdot \overline{\text{Nor}(A, B, C)} \\
 & + \overline{\text{Nand}(A, B, C)} \cdot \overline{\text{Nor}(A, B, C)} \\
 & = A \cdot \bar{B} \cdot \bar{C} + \bar{A} \cdot B \cdot \bar{C} + \bar{A} \cdot \bar{B} \cdot C + ABC
 \end{aligned}$$

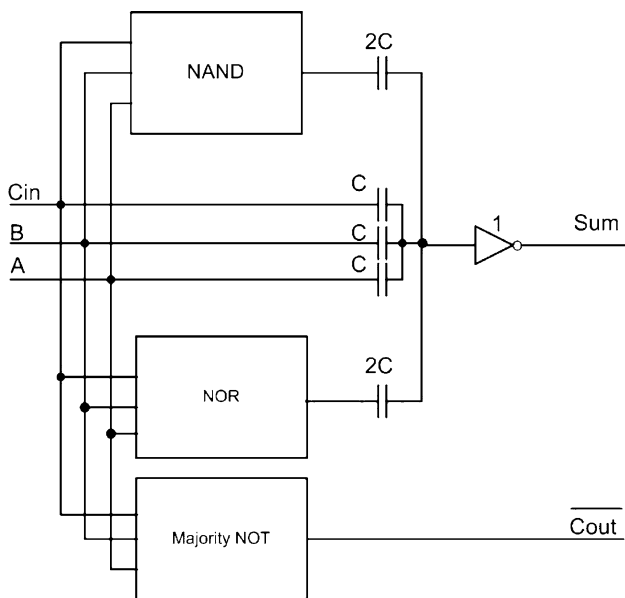


Fig. 3 Schematic of proposed adder

As mentioned before, using a conventional inverter and three capacitors, the majority function is attained and by replacing NAND and NOR gates with three capacitors and an inverter, Fig. 4a will be attained. In view of the fact that three separate capacitors are used for designing each of these gates (9 in total) and that these input capacitors influence the circuit performance by reducing the number of capacitors, the overall performance of the system can be improved. Therefore, we have eliminated six out of the nine capacitors (Fig. 4b, c).

Simulation Results

We compared the proposed design with coeval CNFET Full Adders presented in [12]. To compare these adders, delay, power dissipation and PDP (power-delay product)

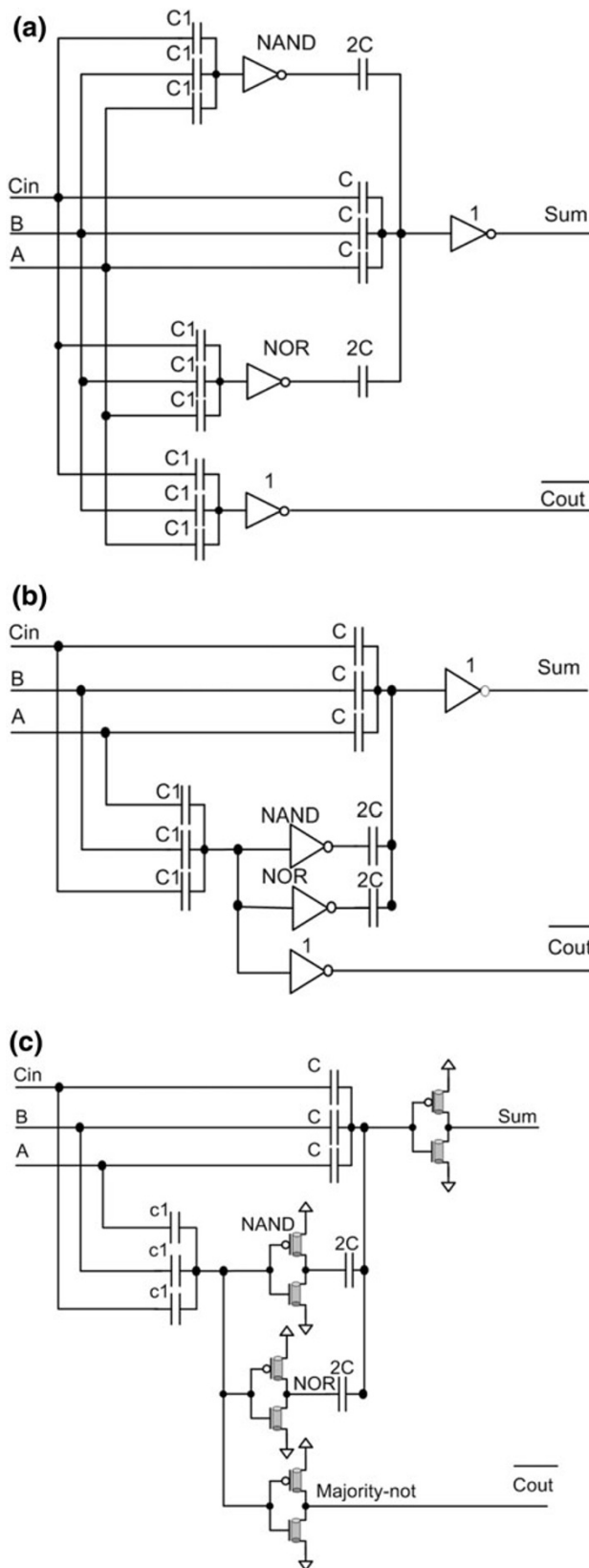


Fig. 4 a proposed adder b optimized proposed adder c final design

Table 1 Simulation results

Design	Power(0.6)	Delay(0.6)	PDP(0.6)
CNFET adder presented in [12] with resistor	1.8567E-06	3.8730E-11	7.1910E-17
CNFET adder presented in [12] without resistor	2.9106E-07	5.0299E-11	1.4640E-17
Proposed Adder	4.6929E-07	2.1369E-11	1.0028E-17

are evaluated. We have measured the delay of the cell from the moment that inputs reach 50% of supply voltage level to the time that the latest of the sum of the signal reach the same voltage level. For being more realistic, we place buffers in the two outputs (two cascaded inverter). Simulations are carried out using HSPICE with CNFET model [2, 3] with the supply voltage at 0.6 V. Table 1 illustrates the achieved values, and among the analyzed adders, the adder in [12], which does not use resistors, consumes less power but has more delay than our proposed adder. As illustrated in Table 1, the proposed Full Adder Cell has the best PDP in comparison to other contemporary Full Adders.

Conclusion

In this paper, a novel high speed Majority-Not (Minority) function-based CNFET Full Adder is proposed. The main idea of this design is a new approach for implementing the SUM output. That is, SUM can be considered as $\text{Minority}(A,B,C,2*\text{Nand}(A,B,C),2*\text{Nor}(A,B,C))$. This adder has a simple design, because it only uses capacitors and inverter in its structure. Simulations are carried out using HSPICE simulator with CNFET model for proposed design. Inverters that are used in the outputs enhance the driving capability of the designs. Simulation results illustrate that we have achieved a significant improvement in terms of Delay and Power-Delay product.

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