

Impacts of Post-metallisation Processes on the Electrical and Photovoltaic Properties of Si Quantum Dot Solar Cells

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Received: 14 June 2010 / Accepted: 15 July 2010 / Published online: 1 August 2010
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Abstract As an important step towards the realisation of silicon-based tandem solar cells using silicon quantum dots embedded in a silicon dioxide (SiO_2) matrix, single-junction silicon quantum dot (Si QD) solar cells on quartz substrates have been fabricated. The total thickness of the solar cell material is 420 nm. The cells contain 4 nm diameter Si quantum dots. The impacts of post-metallisation treatments such as phosphoric acid (H_3PO_4) etching, nitrogen (N_2) gas anneal and forming gas (Ar: H_2) anneal on the cells' electrical and photovoltaic properties are investigated. The Si QD solar cells studied in this work have achieved an open circuit voltage of 410 mV after various processes. Parameters extracted from dark I - V , light I - V and circular transfer length measurement (CTLM) suggest limiting mechanism in the Si QD solar cell operation and possible approaches for further improvement.

Keywords Silicon · Quantum dots · Solar cells · Third generation · Electrical characterisation

Introduction

The concept of a tandem solar cell has been well developed as a method of improving solar cell efficiency. In a tandem cell, solar cells of different band gaps are stacked on top of one another. The cell with the highest band gap is placed on the top, while the cell with the lowest band gap is positioned at the bottom of the tandem stack. Each cell

absorbs the light it can most effectively convert, with the rest passing through to the underlying cells [1]. The highest efficiency cells to date are tandem cells made using single crystal III-V materials. These materials are grown by very expensive epitaxial techniques.

An 'all-Si' tandem solar cell makes use of inexpensive silicon thin-film technology in combination with a high-efficiency multi-band gap approach. It takes the advantage of quantum confinement effects in silicon. When silicon is made very thin (of the order of a few nanometers) in one or more dimensions, quantum confinement causes its effective bandgap to increase. The strongest effect is obtained when silicon is confined in 3D (i.e., quantum dots). If the quantum dots are close to each other, carriers can tunnel between them to form quantum dot superlattices which can be used as the higher bandgap cells in a tandem stack (Fig. 1) [2].

A simple approach to make Si quantum dot super lattices has been described by Zacharias et al. [3]. Similar multi-layer structure was also suggested for the formation of InGaAs quantum dots [4]. The effective bandgap of silicon thin films made this way can be varied by varying the size of the quantum dots. This effect has been supported by photoluminescence (PL) measurements (Fig. 2) [1, 5].

As an encouraging step towards the realisation of silicon-based tandem solar cells using silicon quantum dots embedded in a silicon dioxide (SiO_2) matrix, single-junction silicon quantum dot (Si QD) solar cells on quartz substrates have been fabricated.

We also demonstrate that post-metallisation treatments such as phosphoric acid (H_3PO_4) etching and forming gas (Ar: H_2) anneal significantly impact solar cell performance. So far, our best single-junction Si QD solar cell has achieved 490 mV V_{oc} [6, 7] (In this paper, samples with V_{oc} up to 410 mV are studied). Our medium-term goal is to demonstrate V_{oc} over 700 mV on single-junction Si QD

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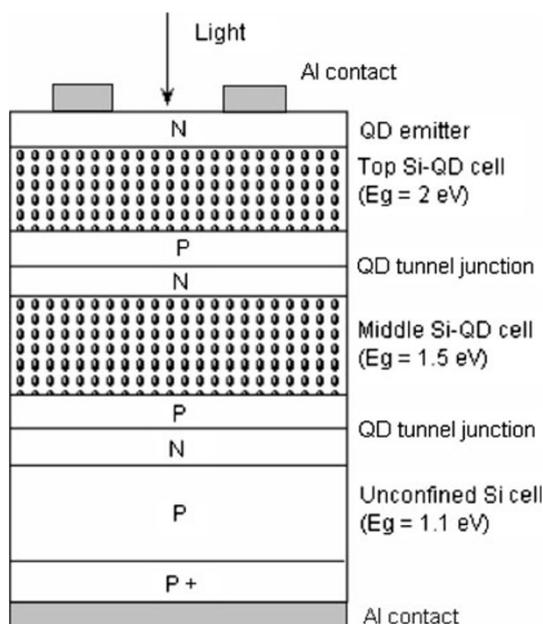


Fig. 1 Schematic diagram of an all-Si quantum dot super lattice tandem solar cell [2]

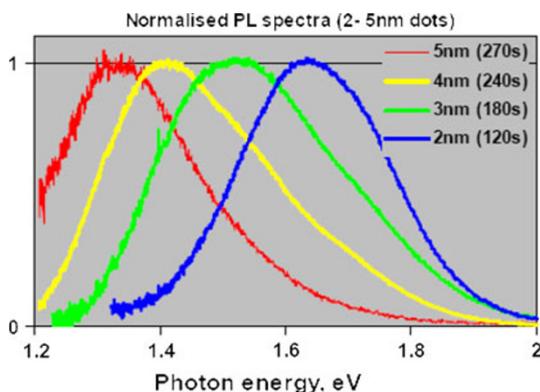


Fig. 2 Normalised photoluminescence for Si QDs of various sizes in SiO₂ matrix [1]

solar cells. As this would be close to the V_{oc} record [8] of single-junction mono-crystalline silicon solar cells, in a thin film solar cell it would be a clear demonstration that the electronic band gap of the nanostructured material is enhanced due to the quantum confinement effect. At present, the emphasis is on increasing V_{oc} and the devices are very unoptimised for absorption and collection. Hence, the very low currents currently obtained are not a concern.

Fabrication of Single-Junction Silicon Quantum Dot Solar Cell on Quartz Substrate

Alternating layers of a 2-nm silicon dioxide (SiO₂) followed by a 4-nm silicon-rich oxide (SRO) are deposited on

a quartz substrate using magnetron co-sputtering of Si and quartz (SiO₂) targets [9]. Either a phosphorous pentoxide for n-type doping or boron for p-type doping is incorporated into the Si-rich material during sputtering of appropriate layers, to obtain a p–n junction after annealing. The sample is then annealed at ~1100°C to form Si QDs and to activate these dopants. Hydrogenation was then performed in a cold-wall vacuum system featuring an inductively coupled remote plasma source (Advanced Energy), using a glass substrate temperature of 600–625°C for 15 min [10, 11].

Formation of metal contacts (metallisation) is done by: (1) thermal evaporation of aluminium, (2) photo-lithography to define mesa areas, (3) CF₄:O₂ reactive ion etching (RIE) to etch the unmasked silicon areas until the underlying n-layer is reached, (4) Al evaporation for self-aligned contacts in the trenches, (5) second photo-lithography to define metal contacts pads, (6) thermal evaporation of Al, (7) Liftoff. The resultant structure is shown in Fig. 3. The cells investigated in this work have areas in the range 2–10 mm².

Removal of localised Aluminium shunts

It was found that one cell was severely shunted after the self-aligned metallisation process. The reason for the shunt is attributed to the localised Al shunting routes between p-type and n-type layers (Fig. 4a) due to the imperfect self-alignment. A forming gas anneal (H₂: Ar, 400°C, 20 min) was performed on the sample after the shunting problem was identified. Dark $I-V$ measurements have shown that the situation of the shunt gets worse with the annealing process (Fig. 4b). This suggests the existence of localised Al shunts lying across the p-type and n-type regions as the annealing improves the contact of the Al shunts to both p- and n-regions of the cell thus shorting the cell more effectively.

To overcome this problem, the cell was immersed in 42.5% H₃PO₄ acid etch (25°–40°C) for 6 min. It has been reported earlier that such a phosphoric acid etch can be

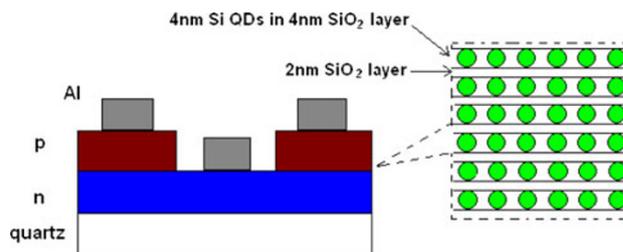


Fig. 3 Schematic diagram of a single-junction Si QD solar cell on quartz substrate. The total thickness of the p–n junction diode is 420 nm. The thickness of the quartz substrate is 1 mm

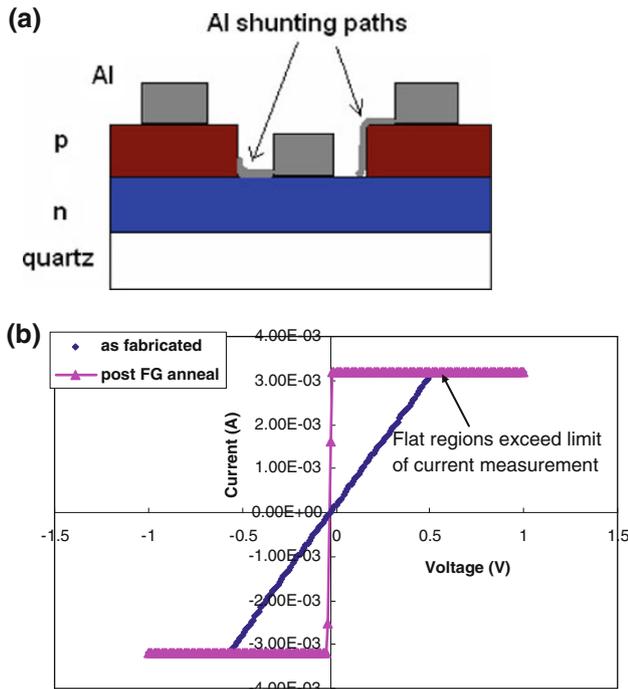


Fig. 4 **a** Schematic diagram of a Si QD cell with localised Al shunts. **b** The corresponding dark I - V curves measured on the shunted cell before and after the forming gas anneal

used to recover shunted polycrystalline thin-film solar cells [12]. This mild chemical etch gradually removes the shunting paths due to the reaction between Al and H_3PO_4 acid. Measurement shows that the solar cell is no longer shunted after the etching (Fig. 5b).

Effects of Nitrogen Gas Anneal and Forming Gas Anneal

Dark and Illuminated I - V Characteristics

Another sample metallised with the aligned photo-lithography method was subjected to an initial N_2 anneal at $250^\circ C$ followed by three consecutive forming gas anneals (250 , 300 and $350^\circ C$). The duration of each annealing step was 20 min. Dark and illuminated (1-sun) I - V data were measured before and after each annealing step.

The dark currents in Figs. 5b and 6a are very different due to the fact that these two devices are metallised in different ways and have different contact geometry. The contacts in the former (sample in Fig. 5b) are made by self-aligned lithography technique which makes the lateral distance between the base and emitter electrodes very small ($<5 \mu m$) but easier to be shunted. On the other hand, the latter aligned lithography approach (sample in Fig. 6a) utilises two separate lithography masks, creating a larger

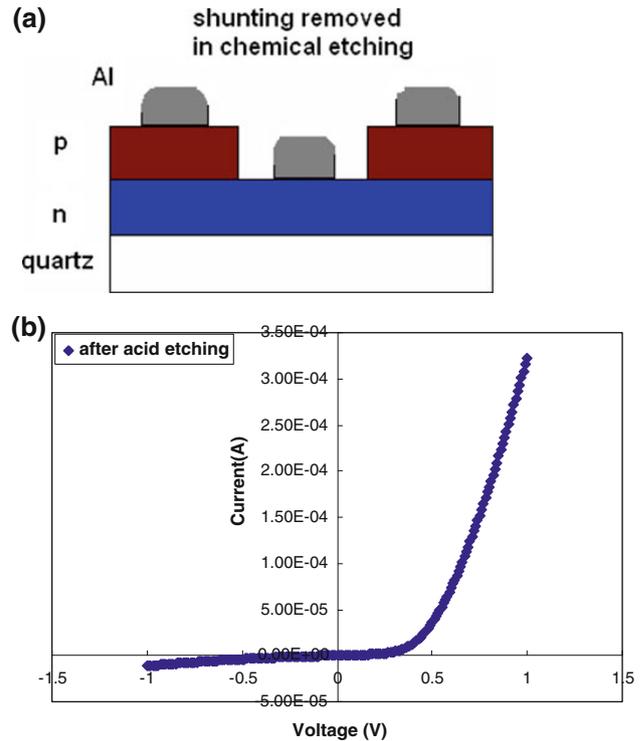


Fig. 5 **a** Schematic diagram of the same cell as in Fig. 4 after H_3PO_4 etching. Local Al shunts are removed. **b** The corresponding dark I - V curve showing rectifying behaviour and a large shunt resistance ($R_{sh} = 2 \times 10^5 \Omega$)

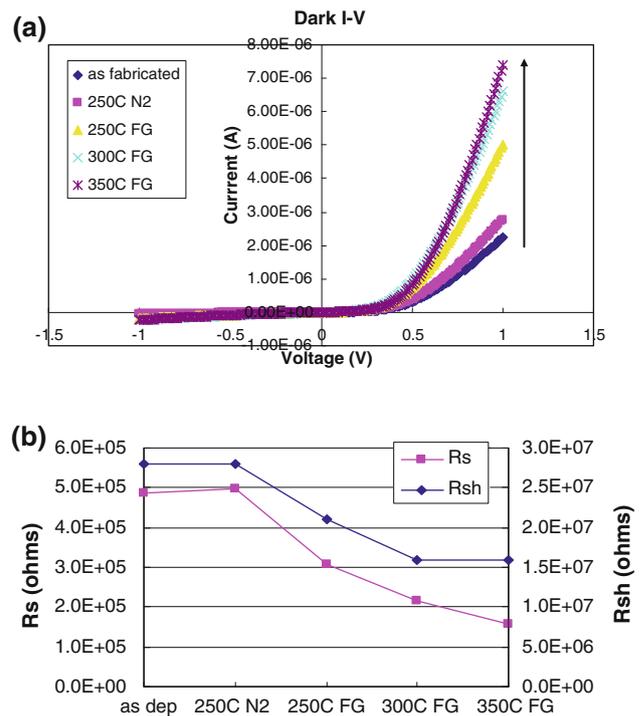


Fig. 6 **a** Evolution of the dark I - V characteristics of the measured cell following initial nitrogen ($250^\circ C$) and consecutive forming gas anneals (250 – $350^\circ C$). **b** R_s and R_{sh} extracted from the dark I - V curves as a function of annealing steps

separation ($\sim 50 \mu\text{m}$) between the base and emitter metal contacts. Given that the resistance of the semiconductor material is very high (as shown in Fig. 8), a larger lateral contact separation makes the overall resistance of the device substantially larger, resulting in a current decrease of two orders of magnitude.

It has been noted that a N_2 gas anneal at 250°C has a very limited influence on the I – V characteristics, while a forming gas anneal at the same temperature is able to alter the electrical properties (Fig. 6). With increasing forming gas annealing temperature, there is a clear change in both dark and light I – V curves. Information about the parasitic resistances (R_s and R_{sh}) is extracted from the dark I – V curve. V_{oc} and I_{sc} are obtained from the light I – V data. Details about the calculation of R_s are discussed in later sections.

The test solar cell with an initial open circuit voltage of 350 mV produces a V_{oc} of 410 mV after the 350°C forming gas anneal step (Fig. 7). The performance of the cell is heavily limited by the series resistance, although the magnitude of the series resistance has been reduced by more than three times after annealing. The shunt resistance has also decreased which might have a detrimental effect. However, this effect is very small as R_{sh} of the cell is in the order of $1 \text{ M}\Omega\cdot\text{cm}^2$. The short circuit current increases by a factor of three due to the decrease of R_s .

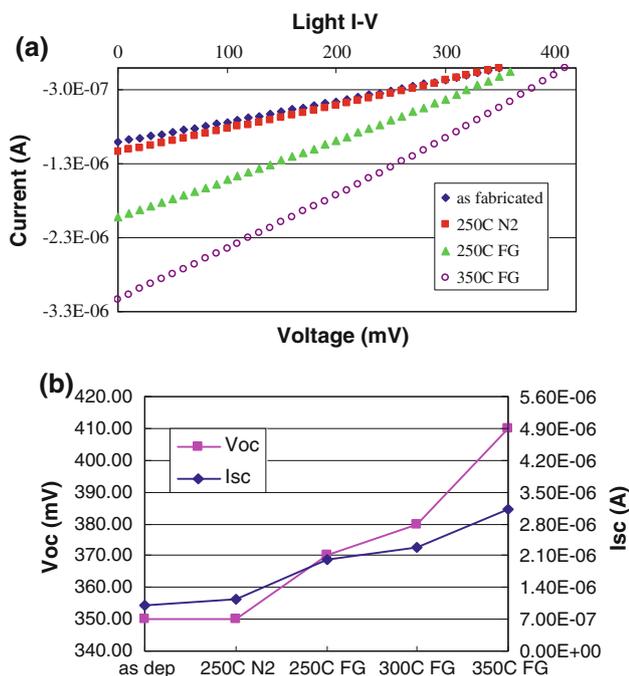


Fig. 7 a The 1-sun light I – V characteristics of the cell. b V_{oc} and I_{sc} extracted from the light I – V curves as a function of annealing conditions

Contact and Sheet Resistances

To identify the origin of the large series resistance, a circular transfer length measurement (CTLM) [13] contact was applied photolithographically to the n-type material and measurements were carried out before and after each annealing step. The measurement is able to extract contact (R_c) resistance of the bottom electrode and sheet (R_{sheet}) resistance of the n-type layer (Fig. 8).

It can be seen from the data that the 250°C N_2 gas anneal has a negative impact on the cell’s contact resistance, while the forming gas anneals improve the contact. The change of sheet resistance is negligibly small when annealed in N_2 ambient. However, annealing in forming gas is able to reduce R_{sheet} by approximately three times. The contact resistance is small in comparison with the semiconductor sheet resistance, as shown in Fig. 8. Therefore, the reduction of series resistance is largely due to the reduction of the material’s resistivity.

The implication of the results is that the H_2 in the forming gas is responsible for the improvement of the cell material. Hydrogen atoms are able to passivate the interfaces of the Si nanocrystals [14] and hence to reduce trap density and facilitate better carrier transport.

Extraction of Series Resistance and Apparent Ideality Factor (n)

Special attention has been paid to the analysis of the series resistance (R_s) of the cell. Instead of simply calculating the slope of the dark I – V curve at the high voltage region, R_s is obtained according to the following.

In a general solar cell circuit model, the total voltage across the terminals (V) equals the voltage across the diode (V_D) plus the voltage across the series resistance (V_{R_s}).

$$V = V_D + V_{R_s} \tag{1}$$

By rearranging the ideal diode equation [15]:

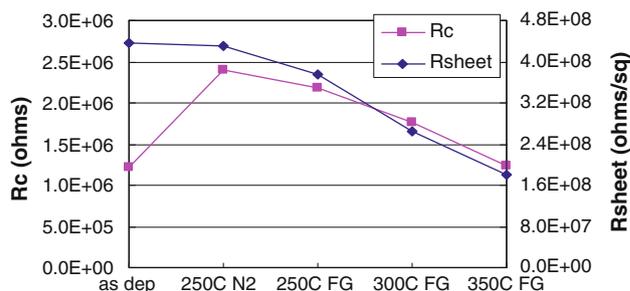


Fig. 8 Contact (R_c) and sheet (R_{sheet}) resistances measured by CTLM

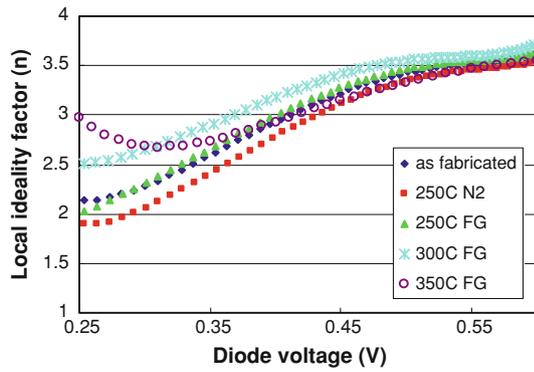


Fig. 9 Ideality factor n calculated from the I - V curves

$$I = I_0 \left[\exp\left(\frac{qV_D}{nkT}\right) - 1 \right] \quad (2)$$

and for $V_D \gg nkT/q$, it can be shown that

$$V_D \cong \frac{nkT}{q} \ln\left(\frac{I}{I_0}\right) \quad (3)$$

Substituting Eq. (3) into Eq. (1), yields

$$V = \frac{nkT}{q} \ln\left(\frac{I}{I_0}\right) + IR_s \quad (4)$$

Differentiating V with respect to I ,

$$\frac{dV}{dI} = \frac{nkT}{qI} + R_s \quad (5)$$

To obtain R_s from the dark I - V data, it is convenient to plot dV/dI against $1/I$ (See Eq.(5)). The plot appears to be a linear relationship. The intercept of the line with the y -axis gives R_s (R_s results are shown in Fig. 6b), while the slope of the line equals to nkT/q . Thus, the ideality factor $n = \text{slope}/V_T$, where $V_T = kT/q$ is the thermal voltage.

The ideality factor (n) extracted for the cells investigated in this work is found to be in the range 2–4 (Fig. 9), with no obvious explanation as to why n should be greater than 2. This may be because the conventional circuit model for a solar cell, which accounts for current flow in only one dimension, is insufficient for modelling a thin-film diode with high base or emitter resistance. An improved circuit model incorporating current crowding effects should be used to describe this behaviour [6].

Conclusions

In this work, we have fabricated single-junction Si QD solar cells on quartz substrates, as an important step to realise an ‘all-silicon’ tandem solar cell.

The impacts of post-metallisation treatments such as phosphoric acid (H_3PO_4) etching, nitrogen (N_2) gas anneal

and forming gas (Ar: H_2) anneal on the cells’ electrical and photovoltaic properties have been studied. The Si QD solar cells investigated in this work have achieved an open circuit voltage of 410 mV after various processes.

Parameters extracted from dark I - V , light I - V and circular transfer length measurement (CTLTM) suggest that the performance of the solar cell is strongly limited by poor carrier transport. This limiting factor can be partly eliminated by forming gas annealing.

Other possible solutions include reduction of the barrier height and thickness of the quantum mechanical tunnelling barrier, modification of the composition of the cell’s absorber material, improved Si QD growth, an improved device structure such as using a transparent conducting contact (e.g. ITO) or a conductive substrate to avoid current crowding.

Acknowledgments The authors gratefully thank all members of the Third Generation Group at the ARC Photovoltaics Centre of Excellence for their contributions to this project. This work is supported by the Australian Research Council (ARC) via its Centers of Excellence Scheme. The authors also acknowledge the support of the Global Climate and Energy Project (GCEP), administered by Stanford University, for helping to fund this work.

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