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Small-area and compact CMOS emulator circuit for CMOS/nanoscale memristor co-design

SangHak Shin[1], Jun-Myung Choi[1], Seongik Cho[2] and Kyeong-Sik Min[1*]

Abstract

In this paper, a CMOS emulator circuit that can reproduce nanoscale memristive behavior is proposed. The proposed emulator circuit can mimic the pinched hysteresis loops of nanoscale memristor memory's current-voltage relationship without using any resistor array, complicated circuit blocks, etc. that may occupy very large layout area. Instead of using a resistor array, other complicated circuit blocks, etc., the proposed emulator circuit can describe the nanoscale memristor's current-voltage relationship using a simple voltage-controlled resistor, where its resistance can be programmed by the stored voltage at the state variable capacitor. Comparing the layout area between the previous emulator circuit and the proposed one, the layout area of the proposed emulator circuit is estimated to be 32 times smaller than the previous emulator circuit. The proposed CMOS emulator circuit of nanoscale memristor memory will be very useful in developing hybrid circuits of CMOS/nanoscale memristor memory.

Keywords: Emulator circuit; CMOS emulator circuit; Memristors; Memristive behavior; Nanoscale memristor memory; CMOS/nanoscale memristor co-design

Background

Memristors are being intensively explored as possible candidate for future memories because of simplicity in fabrication, possibility in three-dimensional integration, compatibility with (complementary metal-oxide-semiconductor) CMOS technology in the fabrication process, and so on. However, real integration of memristors and CMOS circuits is very rarely available to most engineers and scholars who want to be involved in designing various kinds of CMOS circuits using memristors. To help those engineers and scholars who cannot access memristor fabrication technology but want to design memristor circuits, a CMOS emulator circuit that can reproduce the physical hysteresis loop of memristor's voltage-current relationship is needed.

Methods

Before we develop a CMOS emulator circuit for memristor, memristive behavior should be explained first. The following simple equation (Equation 1) can describe the memristor's current-voltage relationship [1,2]:

$$v(t) = R_X(t)\cdot i(t) = \left(R_{SET}\frac{w(t)}{D} + R_{RESET}\left(1-\frac{w(t)}{D}\right)\right)i(t)$$
$$= \left(R_{SET}\frac{q(t)}{Q_{CRIT}} + R_{RESET}\left(1-\frac{q(t)}{Q_{CRIT}}\right)\right)i(t) \quad where$$
$$\frac{w(t)}{D} = \mu_v\frac{R_{SET}}{D^2}q(t) = \frac{q(t)}{Q_{CRIT}}, \text{ and } Q_{CRIT} = \frac{D^2}{\mu_v R_{SET}} \tag{1}$$

Here $v(t)$ and $i(t)$ represent the voltage and current of memristor, respectively. $R_X(t)$ is the memristance that changes with respect to time. R_{SET} and R_{RESET} are SET and RESET resistance, respectively. $w(t)$ is the effective width of the memristor. D is the total drift length of $w(t)$. $q(t)$ is an accumulated charge flow through the memristor. Q_{CRIT} means an amount of critical charge to RESET-to-SET transition. When $q(t)$ becomes equal to Q_{CRIT}, $R_X(t)$ is changed to R_{SET} from R_{RESET}. Here μ_v is the mobility of dopant in Equation 1 [1,2].

To describe the memristive behavior that follows the relationship of current and voltage in Equation 1, a few emulator circuits have already been proposed [3-5].

* Correspondence: mks@kookmin.ac.kr
[1]School of Electrical Engineering, Kookmin University, Seoul 136-702, Korea
Full list of author information is available at the end of the article

Pershin and Ventra proposed an emulator circuit that is composed of an analog-to-digital converter and microcontroller that are implemented by discrete off-chip devices. Thus, they can be considered too much complicated and too large to be integrated in a single chip [3]. Jung et al. proposed an emulator circuit that is based on CMOS technology [4], where a memristor that should change its resistance in response to the applied current and voltage is implemented by an array of resistors. In the emulator circuit with resistor array, the analog-to-digital converter and the decoder circuit select a proper resistor among many resistors that are placed in the resistor array according to the applied voltage or current [4]. One problem in the emulator circuit [4] is that the voltage-current relationship seems sawtooth. This is because the resolution of memristance change is decided by the resolution of the analog-to-digital converter, as you see in [4]. If we have 4-bit analog-to-digital converter in the emulator circuit, it means that only 16 values of memristance are available. As a result, when we apply a voltage that is a sinusoidal function to the memristor, we can know that its current is increased or decreased like sawtooth. To improve the resolution of memristance change, the resolution of the analog-to-digital converter should be increased too. If the resolution of the analog-to-digital converter is improved from 4 to 5 bit, the voltage-current relationship of the emulator circuit with 5 bit seems to be much finer than the emulator circuit with a 4-bit analog-to-digital converter, as shown in [4]. To improve the resolution twice, however, the number of resistors in the resistor array should be double too. It can cause a large area overhead in realizing this emulator circuit in a single chip. Especially, in implementing memristor array with this emulator circuit, this large area overhead of each memristor emulator cell can be a serious problem because each cell in the memristor array should be realized by this large-area single memristor emulator.

To mitigate the large area overhead of the previous emulator circuit, we propose a new emulator circuit of memristors that is more compact and simpler than the previous emulator circuits [6]. The new emulator circuit does not use a resistor array, an analog-to-digital converter, and so on that usually occupy very large area. Instead of using the complicated circuit blocks that were mentioned just earlier, the new circuit can change its memristance value by a simple voltage-controlled resistor that can be realized by a single n-type metal-oxide-semiconductor field-effect transistor (NMOSFET) device.

Newly proposed emulator circuit for describing memristive behavior

A schematic of the proposed emulator circuit for describing memristive behavior is shown in Figure 1. The CMOS circuit for emulating memristive behavior is composed of transmission gates, comparators, current mirrors, voltage-controlled resistor, etc. as shown in Figure 1. V_{IN} is an input voltage source and V_{IN+} and V_{IN-}represent the anode and cathode of the input voltage source, respectively. In Figure 1, V_{IN+} is connected to TG_1 and TG_2 that are controlled by T_B and T, respectively. Similarly, V_{IN-} is connected to TG_3 and TG_4 that are controlled by T and T_B, respectively. When V_{IN+} is greater than V_{IN-}, T becomes high and T_B becomes low, by the comparator G_1. On the contrary, when V_{IN+} is smaller than V_{IN-}, T becomes low and T_B becomes high. Thus, we can know that V_{IN+} is connected to V_A through TG_2 when V_{IN+} is larger than V_{IN-}. At the same moment, V_{IN-} is connected to the ground potential (GND) by TG_3. When V_{IN-} is larger than V_{IN+}, V_{IN-} is connected to V_A through TG_4, and V_{IN+} is biased by GND through TG_1. One thing to note here is that we can deliver the input voltage V_{IN} to V_A without any sacrificial voltage loss, using the transmission gate.

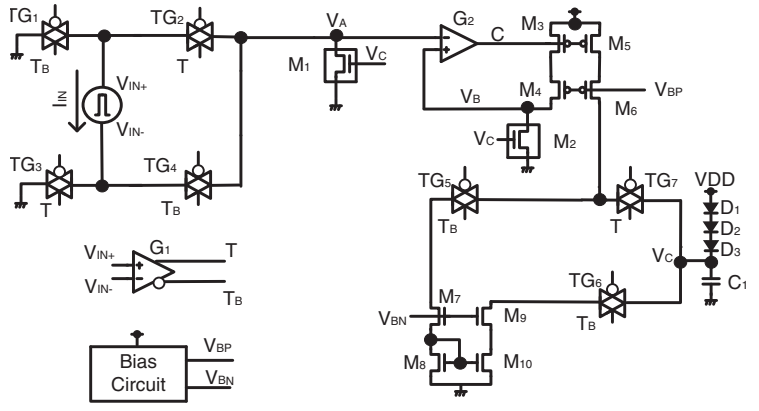

Figure 1 The proposed CMOS emulator circuit for describing memristive behavior.

The V_{IN} delivering block that is composed of four transmission gates, TG_1, TG_2, TG_3, and TG_4, can deliver V_{IN+} and V_{IN-} that are plus and minus polarity of V_{IN}, respectively, to V_A that has only plus polarity, not minus. The delivered voltage V_A is copied exactly to V_B by the negative feedback circuit that is composed of the OP amp, G_2, M_3, and M_4. Using this circuit block, V_B can be the same as V_A by the feedback amplifier with unity gain. V_B is connected to the voltage-controlled resistor M_2 that is controlled by V_C. One more thing to note here is that V_C controls both voltage-controlled resistors M_1 and M_2 that are electrically isolated from each other. By doing so, we can separate the memristor's current from the programming current to change the state variable that is stored at the capacitor C_1. If the memristor's current is not separated from the programming current, the state variable that decides memristance value can be maintained only at the moment when the programming voltage or current is applied to the memristor. If so, the emulator circuit cannot keep its

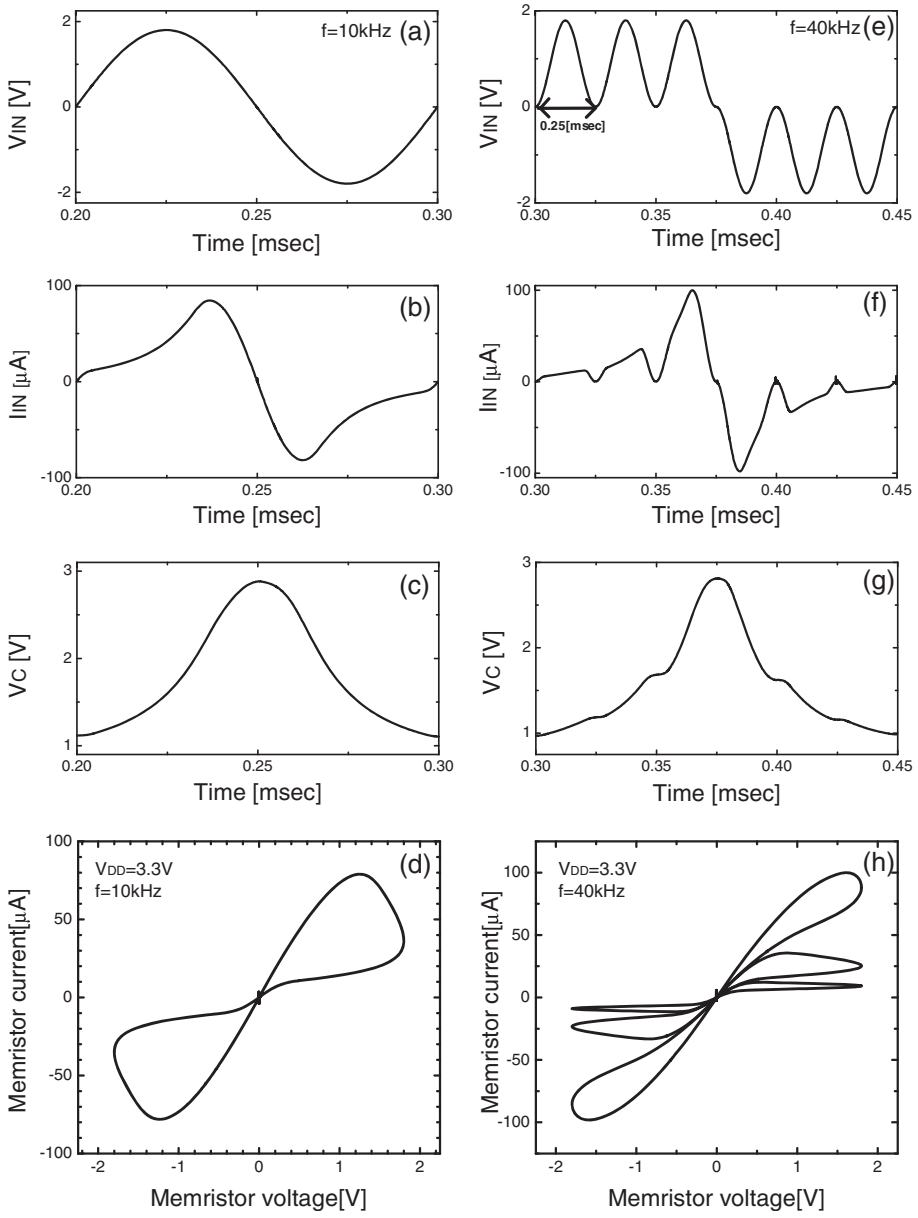

Figure 2 Simulated voltage waveforms. The simulated voltage waveforms of **(a)** V_{IN}, **(b)** I_{IN}, **(c)** V_C, and **(d)** the pinched hysteresis loop of the voltage-current relationship of the proposed emulator circuit when the sinusoidal frequency is 10 kHz. The simulated voltage waveforms of **(e)** V_{IN}, **(f)** I_{IN}, **(g)** V_C, and **(h)** the pinched hysteresis loop of the voltage-current relationship of the proposed emulator circuit when the sinusoidal frequency is 40 kHz.

programmed state variable when the applied voltage or current is removed.

V_C that controls two voltage-controlled resistors M_1 and M_2 acts as a state variable in the emulator circuit that is calculated by an amount of stored charge at C_1. When V_{IN+} is greater than V_{IN-}, TG_7 is on and both TG_5 and TG_6 are off. At this time, the current mirror that is composed of M_5 and M_6 delivers the programming current to C_1 to increase an amount of stored charge; thereby the state variable becomes larger. On the other hand, when V_{IN-} is greater than V_{IN+}, TG_7 is off and both TG_5 and TG_6 are on. By doing so, we can decrease the amount of charge that is stored at the state variable capacitorC_1. The discharging current path is composed of M_7, M_8, M_9, and M_{10} in Figure 1. Here V_{BN} and V_{BP} are the biasing voltages for NMOSFETs and PMOSFETs, respectively. V_{BN} and V_{BP} are made from the biasing circuit that is shown in Figure 1. D_1, D_2, and D_3 are the diodes that are used in the proposed emulator circuit to limit the minimum value of V_C. This minimum value of V_C is needed to avoid the dead zone which may be caused by the sub-threshold region of the voltage-controlled resistors M_1 and M_2. V_D means the diode voltage of D_1, D_2, and D_3. V_{DD} is the power supply voltage of the CMOS emulator circuit in Figure 1.

One more thing to consider here is that the nonlinearity of memristive behaviors can be found when the effective width of memristor, $w(t)$, in Equation 1 becomes much closer to the boundary constraints [1,7]. This nonlinearity near the boundary values of $w(t)$ was introduced in the HP model [1] and mathematically modeled by Corinto and Ascoli [7] to describe various nonlinear behaviors of memristors. In terms of implementation, the diode bridge circuit with LCR filter was proposed to reproduce memristive nature with nonlinearity by using a very simple electronic circuit [8]. In this paper, the window function that is used to define two boundary values of the state variable in the HP model [1] is realized in the CMOS emulator circuit that is shown in Figure 1. The emulator circuit in Figure 1 has two boundary values of the state variable that is defined by V_C. Here we can know that the maximum value of V_C cannot exceed V_{DD}. And also, V_C cannot be lower than V_{DD}-$3V_D$. Thus, the state variable of V_C in Figure 1 can exist only between V_{DD} and V_{DD}-$3V_D$, not being higher than V_{DD} and lower than V_{DD}-$3V_D$, respectively.

Results and discussion

Figure 2a shows the applied input voltage, V_{IN}, to the proposed circuit for emulation of memristive behavior. The voltage waveform is sinusoidal and its frequency and magnitude are 10 kHz and 1.8 V, respectively. The memristor's current I_{IN} that is emulated by the proposed circuit in Figure 1 is shown in Figure 2b. As the sinusoidal voltage is applied to the emulator circuit in Figure 1, I_{IN} changes with respect to time according to the state variable that is represented by V_C, the amount of stored charge at C_1. When V_C has the lowest value, it means that the state variable is in RESET state, where the emulator circuit acts like a memristor with RESET resistance. After the half cycle of sinusoidal function, V_C is charged more and more; thereby V_C can reach the highest value. With the highest value of V_C, the state variable can be in SET state, where the emulator circuit can be considered a SET

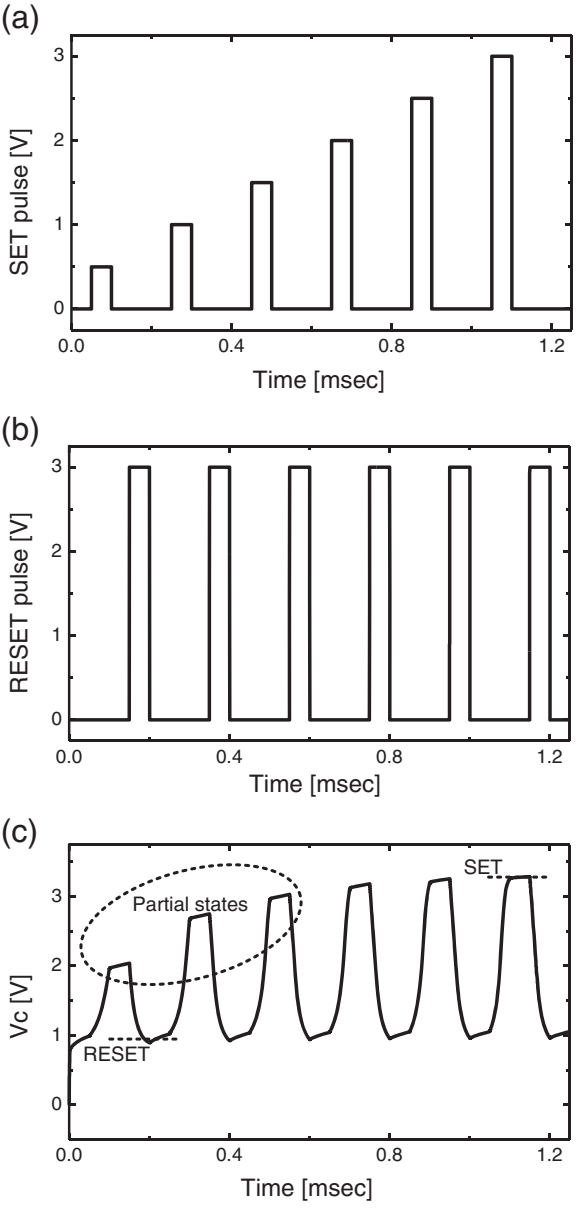

Figure 3 The simulation results of partial states between 'SET' state and 'RESET' state. (a) The voltage waveform of the SET pulse, **(b)** the voltage waveform of the RESET pulse, and **(c)** the voltage waveform of the state variable that is represented by V_C in Figure 1.

resistance. Figure 2c shows the voltage waveform of V_C with respect to time. At the starting point of sinusoidal function of V_{IN}, V_C is 1.2 V that is decided by D_1 in Figure 1. After the half cycle of sinusoidal function, V_C reaches 2.8 V. When one cycle of sinusoidal function is completed, the V_C value returns to the value at the starting point of sinusoidal function. Figure 2d shows a typical pinched hysteresis loop of a memristor's voltage and current which are emulated by the proposed circuit in Figure 1. In the simulation, V_{DD} is 3.3 V and the frequency of sinusoidal function is 10 kHz.

Figure 2e, f, g, h shows the simulation results of the proposed emulator circuit with four times higher frequency of 40 kHz than that of Figure 2a, b, c, d, V_{IN}, I_{IN}, V_C, and the pinched hysteresis loop, respectively, with 10 kHz. A sinusoidal voltage with 40 kHz that is applied to the emulator circuit is shown in Figure 2e. Here the first three peaks are for increasing V_C in Figure 1; thereby, the emulator circuit changes from RESET to SET. The next three peaks are for decreasing the state variable; thus, the emulator circuit can return to RESET. I_{IN} and V_C with the sinusoidal function that is indicated in Figure 2e are

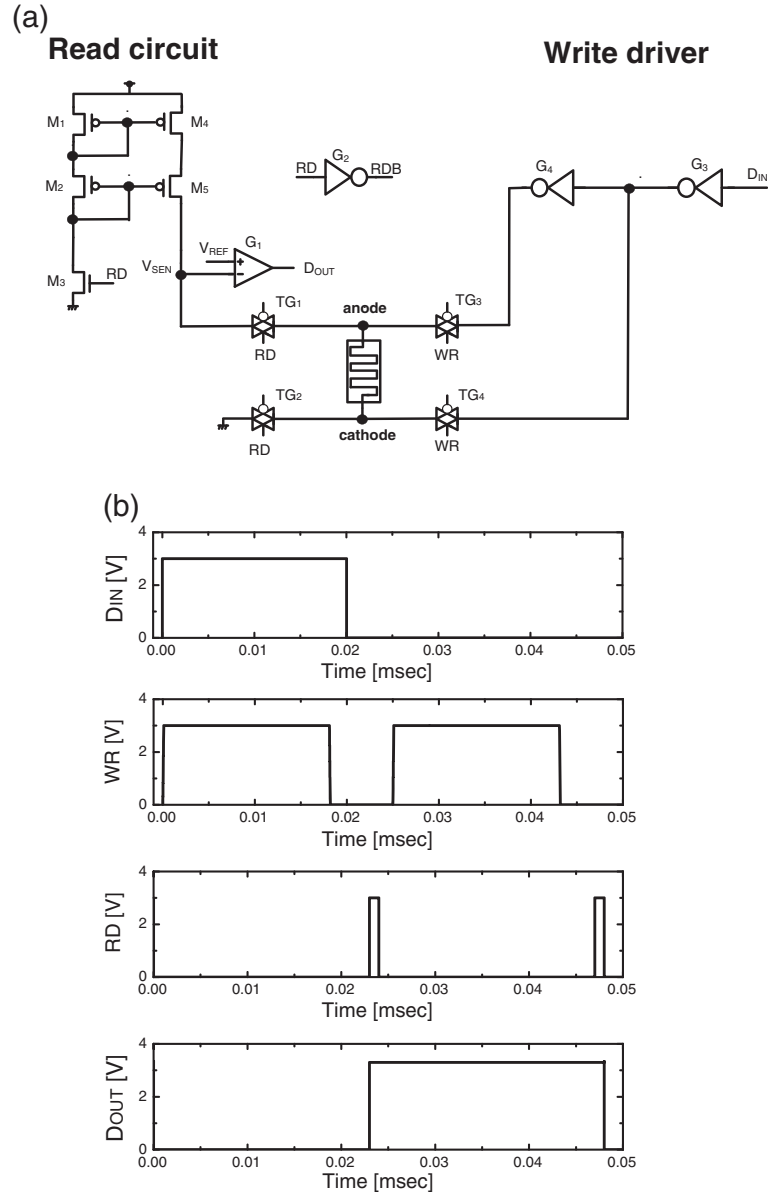

Figure 4 The read and write circuits for the proposed emulator circuit of memristors and the simulated voltage waveforms. (a) The read and write circuits for the proposed emulator circuit of memristors. **(b)**The simulated voltage waveforms of D_{IN}, WR, RD, and D_{OUT} that are the input data of the write driver, write command signal, read command signal, and output data of the read circuit, respectively.

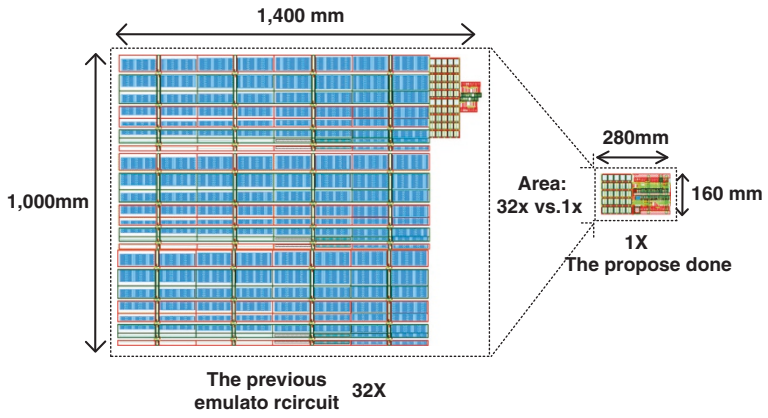

Figure 5 Comparison of layout area between the previous emulator circuit [4] and the proposed emulator circuit. The previous emulator circuit has a layout area as large as 1,400 × 1,000 μm^{2}and the proposed emulator can be placed in an area as small as 280 × 160 μm^2.

shown in Figure 2f, g, respectively. Figure 2h shows the voltage-current relationship of the emulator circuit. In Figure 2h we can see three voltage-current loops at the right and another three voltage-current loops at the left which correspond to the three high peaks and three low peaks in Figure 2e, respectively.

Figure 3a shows SET pulses with different amplitude values. Here the amplitude values are increasing monotonically from 0.5 to 3 V. Each SET pulse is followed by a RESET pulse with the fixed amplitude as high as 3 V that is shown in Figure 3b. The state variable that is changed by SET and RESET pulses are shown in Figure 3c. Here V_C represents the amount of stored charge at C_1 that controls the voltage-controlled resistor in Figure 1 that acts as memristor. Figure 4a shows the read and write circuits for the proposed emulator circuit of memristors [9,10]. The read circuit is simply composed of a current mirror and comparator. The comparator G_1 compares the sensing voltage V_{SEN} with the reference voltage V_{REF}. The sensing voltage V_{SEN} can change according to the programmed memristance value of the emulator circuit. If the state variable is closer to RESET, the sensing voltage V_{SEN} becomes larger due to a large value of memristance. On the contrary, the state variable is in SET, and V_{SEN} is smaller than V_{REF}. Here D_{OUT} is the output voltage of the read circuit. G_2 is the inverter for RD that is the 'read' command signal. TG_1 and TG_2 are the transmission gates for the read operation. When RD is high, TG_1 and TG_2 are on. On the contrary, TG_3 and TG_4 are on for the 'write' operation that is activated by the write command signal WR. The input data D_{IN} drives the inverter G_3. And G_3 drives the next inverter G_4. The anode and cathode of the proposed emulator circuit are driven by the two inverters, G_3 and G_4, respectively. Figure 4b shows the voltage waveforms of D_{IN}, WR, RD, and D_{OUT}.

Figure 5 compares the layout area of the previous emulator circuit [4] and the proposed emulator circuit. Because the resistor array is not used in the proposed circuit and the analog-to-digital converter and decoder are eliminated in this paper, the layout area of the previous emulator circuit is estimated to be 32 times larger than the emulator circuit proposed in this paper. The design rule used in this layout is MagnaChip 0.35-μm technology.

Conclusions

In this paper, a CMOS circuit that could emulate memristive behavior was proposed. The proposed emulator circuit could mimic the pinched hysteresis loops of a memristor's current-voltage relationship without using a resistor array and complicated circuit blocks that may occupy very large layout area. Instead of using a resistor array, other complicated circuit blocks, etc., the proposed emulator circuit could mimic memristive behavior using simple voltage-controlled resistors, where the resistance can be programmed by the stored voltage at the state variable capacitor. Comparing the layout area between the previous emulator circuit and the proposed one, the layout area of the emulator circuit proposed in this paper was estimated to be 32 times smaller than the previous emulator circuit.

Competing interests

The authors declare that they have no competing interests.

Authors' contributions

All authors have contributed to the submitted manuscript of the present work. KSM defined the research topic. SHS and JMC did the simulation and layout. SC provided critical comments on the draft manuscript. KSM wrote the paper. All authors read and approved the final manuscript.

Authors' information

SHS and JMC are M.S. students who are studying at the School of Electrical Engineering, Kookmin University, Seoul, Korea. SC is a professor at the Division of Electronics and Information Engineering, Chonbuk National University, Jeonju, Korea. KSM is a professor at the School of Electrical Engineering, Kookmin University, Seoul, Korea.

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Author details
[1]School of Electrical Engineering, Kookmin University, Seoul 136-702, Korea.
[2]Division of Electronics and Information Engineering, Chonbuk National University, Jeonju 561-756, Korea.

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