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Junctionless ferroelectric field effect transistors based on ultrathin silicon nanomembranes

Ronggen Cao¹, Gaoshan Huang¹, Zengfeng Di², Guodong Zhu^{1*} and Yongfeng Mei^{1*}

Abstract

The paper reported the fabrication and operation of nonvolatile ferroelectric field effect transistors (FeFETs) with a top gate and top contact structure. Ultrathin Si nanomembranes without source and drain doping were used as the semiconducting layers whose electrical performance was modulated by the polarization of the ferroelectric poly (vinylidene fluoride trifluoroethylene) [P(VDF-TrFE)] thin layer. FeFET devices exhibit both typical output property and obvious bistable operation. The hysteretic transfer characteristic was attributed to the electrical polarization of the ferroelectric layer which could be switched by a high enough gate voltage. FeFET devices demonstrated good memory performance and were expected to be used in both low power integrated circuit and flexible electronics.

Keywords: Silicon nanomembrane; Ferroelectric polymer; Ferroelectric field effect transistor; Junctionless

Background

In the past few years, with the development of silicon-on-insulator (SOI) process techniques [1], Si nanomembranes (SiNMs) have attracted much attention due to their unique properties, such as piezoelectric effect and high speed carrier mobility, and thereof potential applications in flexible electronics [2-6]. SiNM-based devices can be built on one or both sides, which are more immune to short-channel effects and have advantages such as faster and lower voltage/power operation and the compatible manufacturing process with current integrated circuit [7-11]. As we know, nonvolatile memories are a kind of critical microelectronic devices, among which ferroelectric memories have shown large potential especially in flexible nonvolatile memories based on ferroelectric polymer and oxide [12] or organic [13] semiconductors. However, till now, few works have been reported on SiNM-based nonvolatile memories, though such devices are expected to effectively reduce device dimensions, catch up with modern integrated circuit process, and overcome the obstacle in fabricating an ultrashallow junction for 'gated resistors' [14,15]. Here, we report the feasibility and operation of SiNM-based ferroelectric field effect transistor (FeFET) memories.

Methods

The device structure is shown as the inset in Figure 1a. The original SiNMs with a boron doping level of 10^{15} cm^{-3} (part of SOI wafer with Si/SiO₂ thickness of 50/150 nm) were bought from SOITEC Inc. (Bernin, Isère, France), and the TEM cross-section images of SiNM are shown in Figure 1c,d. Al electrodes (100 nm thick) were first deposited onto SiNMs by electron beam evaporation with a hard mask to form source and drain patterns with a channel length of 80 μm and a width of 1 mm. The source and drain were not further implanted. Then, a 10-nm thick Al₂O₃ buffer layer was deposited by atomic layer deposition. Ferroelectric poly (vinylidene fluoride trifluoroethylene) [P(VDF-TrFE)] copolymer films with VDF/TrFE molar ratio of 77/23 were spin-coated onto the Al₂O₃ layer and then annealed at 138°C for 5 h to increase their degree of crystallinity. The thickness of annealed ferroelectric films was about 100 nm, determined by a scanning probe microscope (UltraObjective, Surface Imaging Systems, Herzogenrath, Germany). Finally, 100-nm thick Al electrodes were thermally evaporated to form the gate electrode. Electrical measurements were performed in a dark environment by probe method with Keithley 4200 semiconductor parameter analyzer (Keithley Instruments Inc., Cleveland, Ohio, USA), as shown in Figure 1b. During all electrical measurements, the source electrode was electrically grounded.

* Correspondence: gdzhu@fudan.edu.cn; yfm@fudan.edu.cn

¹Department of Materials Science, Fudan University, Shanghai 200433, People's Republic of China

Full list of author information is available at the end of the article

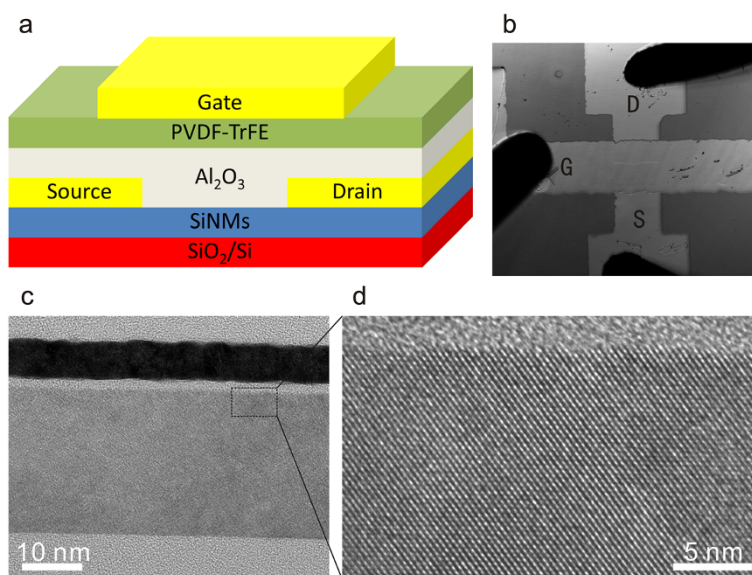


Figure 1 Schematic, optical microscope image, and TEM cross-section images. (a) Schematic of SiNM-based FeFET devices, (b) Optical microscope image of the electrical measurements by probe method, and (c, d) TEM cross-section images of SiNMs.

Results and discussion

The output characteristics of the SiNM-based FeFETs are shown in Figure 2a. The source-drain voltage (V_{ds}) was swept from 0 to 3 V, while the gate voltage (V_g) changed between +4 and -4 V. A typical output characteristic of SiNM-based field effect transistors is observed. The source-drain current (I_{ds}) is hard to be saturated at positive V_g , though the maximum V_{ds} is set to 3 V. This should be due to the fact that the substrate is not electrically grounded and the potential of the SiNMs increases when the current flows through the PN junction of the drain, causing the increase of the channel conductance.

Transfer characteristics of our FeFETs were determined by sweeping V_g between ± 8 V at a constant V_{ds} of 0.5 V. To well-illuminate the experimental results, we define two V_g scanning directions: forward scan corresponds to V_g sweeping from negative to positive voltage, while backward scan corresponds to V_g from positive to negative voltage. Different from the typical metal-oxide-silicon field effect transistors, in which both transfer curves from the forward and the backward scans follow nearly the same trace, the FeFETs show significant hysteresis during transfer measurements (Figure 2b) due to the insertion of the ferroelectric P(VDF-TrFE) film between the gate and the oxide layers. The transfer loop in Figure 2b shows the device's on/off ratio of about 10^2 and the width of memory window of 0.75 V, which is defined as the gap of V_g when I_{ds} is half of its maximum value in a complete hysteresis loop. Furthermore, when the gate voltage is lower than 2.0 V, the gate leakage current I_{gs} is on the order of 10^{-8} A, about 2 orders of magnitude lower than I_{ds} . During the electrical measurements

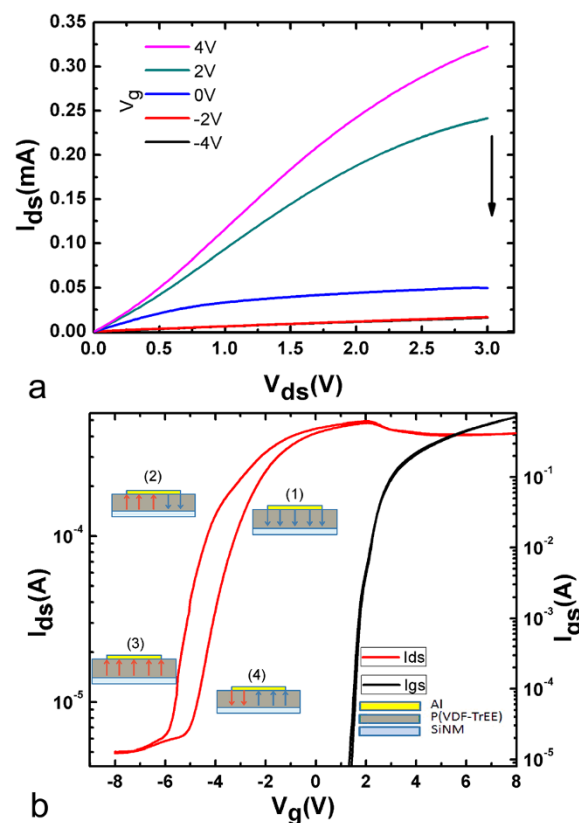


Figure 2 Output and transfer and leakage characteristics of SiNM-based FeFETs. (a) Output and (b) transfer and leakage characteristics. Insets show the schematic diagram of operation mechanism.

by probe method, the mechanical stress applied by the probes causes the compression of the insulating layers between gate and source/drain electrodes and thus decreased film thickness results in the increased leakage current I_{gs} between gate and source, as is also shown in the leakage current curve of Figure 2b. With the further increase of V_g from 2 to 8 V, the leakage current quickly increases from 10 nA to 0.7 mA. The increased leakage current partly counteracts the further increase of I_{ds} especially at a gate voltage larger than 2 V and thus results in the decrease of I_{ds} with further increased gate voltage.

Note that both output and transfer characteristics indicate our FeFETs have a typical n-channel depletion mode (NNN), though the device is based on p-doped silicon without special source and drain doping. Here, the n-channel depletion mode is due to aluminum-silicon interaction. The work function of aluminum and electron affinity of silicon are 4.2 and 4.01 eV, respectively. At the Al/Si interface, the separation between the Fermi level and conduct band is only 0.27 eV (<1.12 eV/2), resulting in the change of the type of the silicon to n-type near the interface. At the same time, the channel is changed to n-type by fixed charges in the gate oxide. The same experimental observation was also reported in a similar Al/Si device structure [5].

The insets in Figure 2b schematically explain the origin of the electrical hysteresis (i.e., memory window) induced by the bistable orientation of electrical dipoles in the ferroelectric layer. These well-oriented dipoles induce a built-in voltage (V_{in}) which causes the shift of the threshold voltage (V_{th}) in the semiconducting layer [12]. Note that voltage drop on the ferroelectric layer larger than the coercive voltage (approximately 4.8 V) can lead to re-orientation of the electrical dipoles. During the backward scan, the initial applied gate voltage of +8 V is high enough to cause polarization reversal in the ferroelectric layer with electrical dipoles aligning downwards to the SiNM (inset 1), which contributes positive V_{in} to the SiNM layer and thus results in a V_{th} shift toward the negative voltage. On the other hand, during the forward scan, the initial applied voltage of -8 V induces the re-orientation of the dipoles aligning against the SiNM layer (inset 3), causing a V_{th} shift to the positive voltage. The insets 2 and 4 schematically show the orientation of the electrical dipoles during V_g sweeping, which correspondingly causes the tuning of V_{in} and then V_{th} . As a result, a hysteresis loop can be expected as shown in Figure 2b.

To present a complete view of the electrical properties in the current devices, we also measured the transfer characteristics at various V_{ds} and noticed that V_{ds} had significant influence on the memory window, especially the device's on/off ratio. The change of the transfer loops with V_{ds} is shown in Figure 3a, where gate voltage

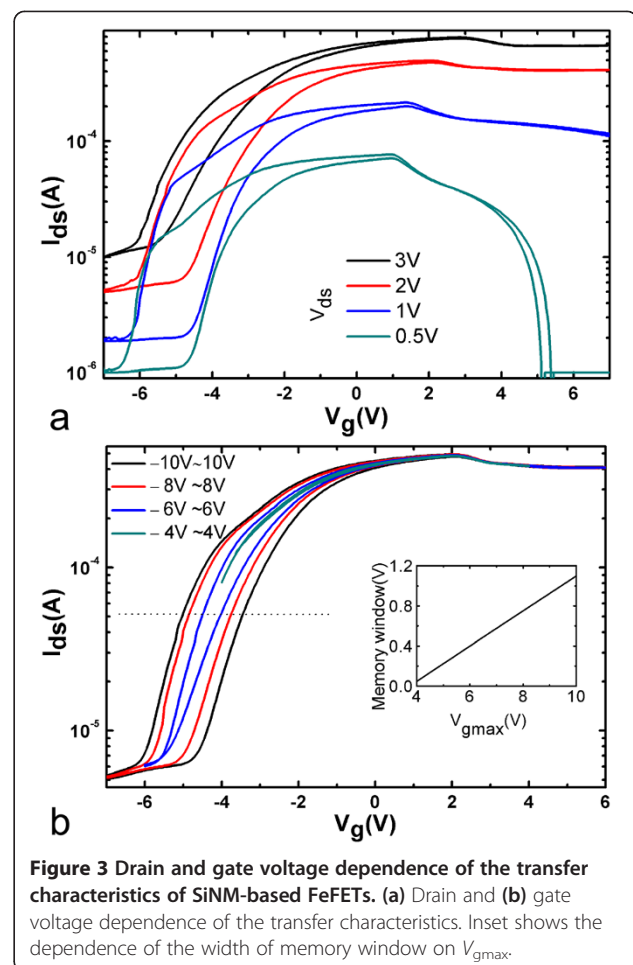


Figure 3 Drain and gate voltage dependence of the transfer characteristics of SiNM-based FeFETs. (a) Drain and (b) gate voltage dependence of the transfer characteristics. Inset shows the dependence of the width of memory window on V_{gmax} .

was swept between ± 8 V. The width of memory windows almost remains constant at about 0.75 V, regardless of V_{ds} values. However, the device's on/off ratio reduces significantly from 10^2 to 10^1 with the decrease of V_{ds} from 3 to 0.5 V.

Gate voltage determines the polarization in the ferroelectric layer and thus influences the memory window. To explore the mechanism behind this, we carried out more electrical characterizations on our devices. We determined the influence of V_{gmax} on the memory window, where V_{gmax} was the applied maximum gate voltage during one measurement of a whole hysteresis loop. Typical results are shown in Figure 3b, where V_{ds} was fixed at 3 V and V_g was swept between $\pm V_{gmax}$. Obviously, the width of the memory window increases with V_{gmax} , and the device's on/off ratio shows negligible change when V_{gmax} is larger than 6 V. The inset in Figure 3b demonstrates the relationship between window width and V_{gmax} : in our experimental condition, window width increases linearly from 0.05 to 1.1 V with the increase of V_{gmax} from 4 to 10 V, indicating more dipole switching and thus larger V_{in} with the increase of V_{gmax} .

Retention performance is especially important for non-volatile memories, which determines the lifetime of the recorded data. Usually, as for nonvolatile memories, retention characterization should be conducted at 0-V gate voltage to meet the nonvolatile requirement. So here, the retention characteristic of SiNM-based FeFETs was measured by first applying writing gate pulses with a duration of 100 s and amplitude of 10 and -10 V and then recording I_{ds} at $V_g = 0$ V and $V_{ds} = 1$ V, respectively, at preset time points. Typical results are shown in Figure 4, where I_{ds} values in both ON and OFF states are plotted as a function of time. Here the ON state corresponds to that written by the +10-V gate pulse while the OFF state to the -10-V pulse. During the writing processes, ON and OFF state currents keep constant at 0.26 and 0.206 mA, respectively. Once the gate pulse is removed, the ON state I_{ds} sharply decreases to 0.23 mA within 130 s and then keeps nearly unchanged in the following 770 s. This sharp decrease of ON state current may be attributed to the depolarization in the ferroelectric layer due to the lack of charge compensation during the application of positive gate voltage, which is considered as one of the main causes of the worse retention performance in ferroelectric field effect transistors [16,17]. On the other hand, the OFF state I_{ds} slightly decreases to 0.203 mA after the removal of the gate pulse and then keeps constant. In the whole retention measurement, the separation between ON and OFF state current decreases from 54 to 27 μ A and the ON and OFF states can still be well distinguished. Especially after the sharp decrease of ON state current in the initial 130 s, both ON and OFF states maintain their currents

well, indicating that the SiNM-based FeFETs exhibit good retention performance.

Note that, in our measurements of transfer characteristic, the whole hysteretic loops shift to the negative gate voltage, as shown in Figures 2b and 3. Such a shift is not due to the built-in voltage caused by the orientation of electrical dipoles in the ferroelectric layer, but due to space charges trapped in the ferroelectric layer and/or the interface between the ferroelectric and its adjacent layers, i.e., imprint effect [18], which is actually quite common in ferroelectric films and devices [19]. Nevertheless, this shift reduces the memory window measured at $V_g = 0$ V, resulting in a low on/off ratio of only 1.14 in the retention measurements in Figure 4. In fact, as for the transfer loop shown in Figure 2b, the maximum on/off ratio of 6.3 occurs at a V_g of -4.8 V, while the maximum separation of 0.11 mA between the ON and OFF state I_{ds} values occurs at a V_g of -3.6 V. To get even better memory performance especially at a V_g of 0 V, further measures should be taken to inhibit space-charge-induced shift in transfer measurements.

Although the SiNM-based FeFET device has been fabricated with good memory performance, the device needs to be further optimized. First, compared with the bulk Si, SiNM with a low doping concentration provides fewer carriers to be modulated by the ferroelectric layer, resulting in a lower switching ratio. In order to achieve good FET characteristics, SiNMs should be heavily doped [20]. Second, SiNMs should be even thinner to obtain a high on/off ratio due to easier gate control [21]. Third, SiNMs can be transferred to flexible substrates and thus flexible 'junctionless' FeFETs can be expected [22].

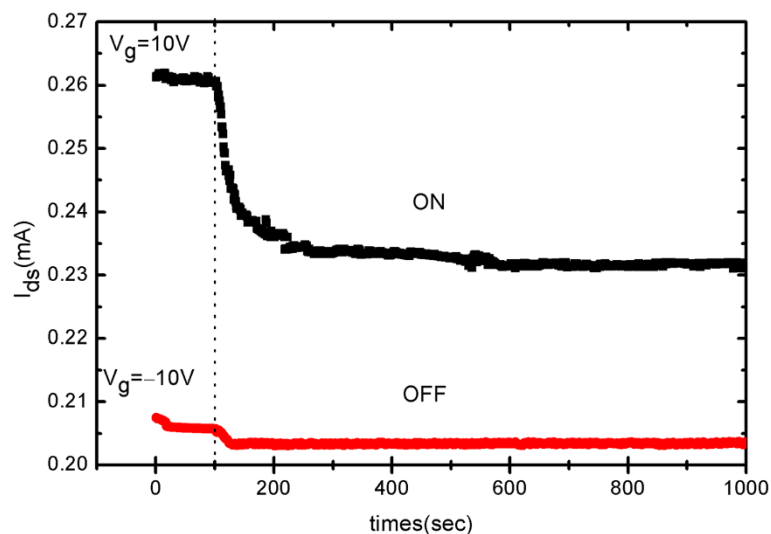


Figure 4 Retention characteristic of the SiNM-based FeFETs. ON and OFF states were written by 100-s pulses with amplitudes of 10 and -10 V, respectively.

Conclusions

In summary, nonvolatile SiNM-based FeFETs have been fabricated by integrating ferroelectric polymer thin films and ultrathin SiNMs. Electrical characterizations show that such devices have hysteretic transfer characteristic due to the modulation of electrical polarization in the ferroelectric layer. The devices show good memory performance with the device's on/off ratio up to 10^2 and memory window width as high as 1.1 V. Such SiNM-based FeFETs exhibit good retention performance and are expected to be used in low power integrated circuit and flexible electronics.

Competing interests

The authors declare that they have no competing interests.

Authors' contributions

RC carried out the whole experimental work and the writing of this manuscript. GH and ZD provided the insightful comments regarding the experimental observations. GZ and YM were in charge of designing and supervision of the experiments. All authors read and approved the final manuscript.

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Author details

¹Department of Materials Science, Fudan University, Shanghai 200433, People's Republic of China. ²State Key Laboratory of Functional Materials for Informatics, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai 200050, People's Republic of China.

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